# CAD Design of Digital VLSI Systems


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**Abstract:**

This course is an introduction to VLSI design. Although the emphasis is on digital VLSI circuits, an initial overview of the analog basis of digital VLSI circuits will be given. Using a state-of-the-art CAD environment provided by CADENCE Design Systems, the students will design combinational and sequential circuits at various levels of abstraction.


**Course Outline:**

First a brief discussion of the device physics of MOSFETs will be presented. Next, CMOS circuits will be used to construct digital primitives such as NOT, NAND, NOR, FLIP-FLOP etc ... These circuits will be analyzed using hand calculations and SPICE/SPECTER simulations. Subsequently, the integration of these primitives using the SCMOS design rules provided by MOSIS will be discussed. A brief overview of the fabrication steps and justifications for the rules will also be provided. Schematic versus layout verification and SPICE simulation will be used to confirm the integrity of the mask layout. Next the behavioral abstraction of the circuits using VERILOG HDL will be developed. The behavioral model will include the effects of the parasitic components encountered in the layout process. Using the behavioral models, a large system will be developed for the class project. The project, which will be defined later, will be integrated into a TINY Chip in 45nm CMOS process. The entire chip will be simulated, verified and converted to GDS for possible submission for fabrication.

**Textbooks:**

Digital Integrated Circuits (2nd Edition), J. Rabaey, 2003, ISBN 0-13-090996-3

**Recommended:**

Verilog HDL: A guide to digital design and synthesis, S. Palnikar, 1996, ISBN 0-13-451675-3

Computer Systems Architecture, M. Mano, 1995, ISBN 0-13-175563-3

**Other References:**


Basic VLSI Design, D. Pucknell and K. Eshraghian 1988

Fundamentals of CMOS VLSI Design, J. Uyemura, 1988

Analysis and Design of Analog integrated Circuits, P. Gray and R. Meyer, 1994
Modern VLSI Design, Wayne Wolf, 1994

**CAD:**

CADENCE SPICE VLSI circuit simulators
SPECTER VLSI circuit simulators
VERILOG-XL Logic/VHDL simulator CADENCE Design Tools for complete design integration, verification and submission in GDS format

**Material Covered:**

Device Physics of MOSFETS, Intro. to Cadence Design Environment, Introduction to Layout and VerilogHDL, The inverter, Combinational Logic, Sequential Logic, Current Issues in Computer Design, Arithmetic Building Blocks, Memory and Arrays